# Method to pattern etch masks in two inclined planes for three-dimensional nano- and microfabrication

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The authors present a method to pattern etch masks for arbitrary nano- and microstructures on different, inclined planes of a sample. Our method allows standard CMOS fabrication techniques to be used in different inclined planes; thus yielding three-dimensional structures with a network topology. The method involves processing of the sample in a first plane, followed by mounting the prepared sample in a specially designed silicon holder wafer such that the second, inclined plane is exposed to continued processing. As a proof of principle we demonstrate the fabrication of a patterned chromium etch mask for three-dimensional photonic crystals in silicon. The etch mask is made on the 90° inclined plane of a silicon sample that already contains high aspect ratio nanopores. The etch mask is carefully aligned with respect to these pores, with a high translational accuracy of $<30$ nm along the $y$-axis and a high rotational accuracy of 0.71° around the $z$-axis of the crystal. Such high alignment precisions are crucial for nanophotonics and for sub-micrometer applications in general. Although we limit ourselves to processing on two planes of a sample, it is in principle possible to repeat the presented method on more planes. The authors foresee potential applications of this technique in, e.g., microfluidics, photonics, and three-dimensional silicon electronics. © *2011 American Vacuum Society*. [DOI: 10.1116/1.3662000]

## I. INTRODUCTION

The fabrication of three-dimensional (3D) devices with very small features by using semiconductor micro- and nanofabrication techniques has been the subject of extensive research. Challenging and very diverse structures have been realized using a large variety of techniques, for examples see Refs. 1–4. An important requirement for many 3D nanostructures is that they have a network topology, meaning that each of the constituent materials is connected everywhere, that is, there are no isolated inclusions present in the structure.[5] However, the directionality of most micro- and nanofabrication techniques impose limitations on the shape or size of the structures that can be designed, in particular regarding CMOS compatible methods. Most of these techniques involve the structuring of planes from one direction, and thus are in essence planar. Certain 3D structures can be formed by underetching and the subsequent deposition of new materials.[6,7] Another example is the fabrication of multilevel structures,[8,9] that can be used to obtain relatively simple 3D structures without buried features. Each subsequent level of the multilevel structures suffers from limitations imposed by the geometry of the previous level(s). Furthermore, the resulting structures have no network topology.[5]

In order to lift the limitations that one-directional processing poses on the 3D structures that can be fabricated, a way of exposing structures to micro- and nanofabrication techniques from more than one plane is necessary. Such a technique is particularly useful to fabricate intricate three-dimensional structures that are interconnected; for example in microfluidics,[10,11] optical devices,[12] and silicon electronics.[13] Figure 1 shows an illustration of a chip we propose, which contains two integrated circuits on two different inclined planes of a silicon sample. This chip could be realized by our multiplanar structuring method. Making 3D chips in this way can greatly increase the density of electrical components in a surface mounted device. It also allows for more and different ways to interconnect the different electronic and microfluidic circuits that are present on the device, and it allows the introduction of sensing- or cooling microfluidic channels for enhanced functionality.[6]

Structuring samples from different directions has been attempted before, notably for nanophotonics. In many studies, focused ion beam milling of very deep pores was used, often in combination with other techniques, to realize

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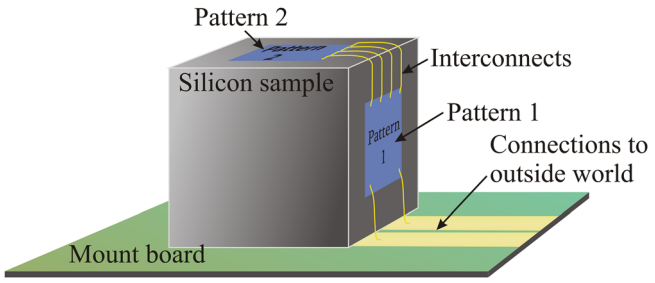


FIG. 1. (Color online) Schematic drawing of a proposed structure consisting of an integrated circuit with Pattern 1 and Pattern 2, fabricated on two 90° inclined planes on a silicon chip. In this way the component densities of chips can be greatly increased, as well as the interconnection options between the various ICs, and sensing- or cooling microfluidic channels can run parallel to both planes of the chip. Our etch mask patterning method allows one to realize such intricate structures.

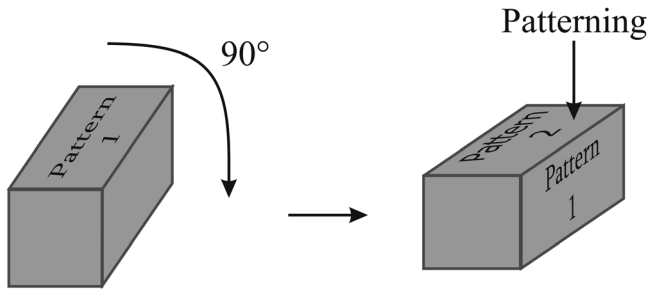


FIG. 2. Schematic illustration of the fabrication process for patterning two inclined planes of a sample. The sample, which already contains structures, is turned on its side and patterned a second time.

three-dimensional structures in silicon,[14,15,17] or in gallium phosphide.[16] Unfortunately, because a focused ion beam can only mill on one spot at a time, focused ion beam milling is a very time-consuming process and therefore not suited for high-volume processing of wafers. In addition, the obtainable aspect ratio of the pores is low compared to the aspect ratios obtainable with modern plasma etching techniques,[24] due to the high degree of redeposition that occurs during milling.[16]

Several groups have been searching for parallel fabrication methods such as plasma etching in more than one direction for the fabrication of 3D nano structures. With parallel fabrication methods all structures can be formed simultaneously, which greatly reduces the fabrication time. Takahashi *et al*. have etched silicon in two orthogonal directions at 45° to the normal of the wafer using reactive ion etching with one and the same etch mask.[18] The wafers were placed in the etching apparatus at an angle. Etching under an angle limits the consistency of the quality of the pores over the entire wafer, since not all etch mask openings that define the pores are etched from the same height in the plasma, which influences the etching rate and -behavior.[19] Furthermore, because one and the same etch mask is used for etching in both directions, the diversity of three-dimensional structures that can be made using this technique is limited.

Here, we present a method to deposit and pattern etch masks on several inclined planes of a sample using standard CMOS silicon micro- and nanofabrication techniques. This method greatly increases the number of available options in making three-dimensional structures. The method can be used for many different ways of etch mask application and -patterning, such as e-beam lithography,[20] laser interference lithography,[21] and deep UV lithography.[22] As a demonstration we show how to realize a chromium etch mask on the inclined plane of a nanostructured silicon sample with deep nanopores. To this end, we apply a chromium layer to a side face of the sample. The chromium was patterned using a focused ion beam, yielding an etch mask in an inclined plane that is suitable for plasma etching to obtain a three-dimensional structure.

## II. PROCESS SCHEME

In order to pattern two inclined planes of a sample, it is necessary to rotate, hold and align the sample. In Fig. 2 the process is shown schematically. The sample that was patterned and processed on one plane (pattern 1) is rotated by an angle, in this case 90°. Subsequently, this 90° inclined plane of the sample can be patterned with a second pattern (pattern 2). A holder has been designed and made to carry out this process reliably and to allow the sample to remain aligned despite the mechanical forces that may occur during further processing.

Figure 3 shows the complete process scheme to pattern a sample on two inclined planes. In Fig. 3(A) the holder, a bare wafer containing slots, is placed on a bare silicon or glass wafer, called the "bare wafer." Samples that will be patterned on an inclined plane are placed in the slots in the holder [Fig. 3(B)]. The use of the bare wafer ensures that the second, inclined plane of the samples is parallel with the holder surface, which allows lithography on that particular plane. A third wafer, containing a thick layer of photoresist, called the "glue wafer," is then placed on the combination of bare wafer, holder and samples [Fig. 3(C)]. The photoresist acts as a glue to fix the samples in the holder. After curing the photoresist, the bare wafer is removed and the combination of the glue wafer and the holder containing the samples is rotated by 180° [Figs. 3(D) and 3(E)]. In the next step the samples are covered with a material for the etch mask that is subsequently patterned [Figs. 3(F) and 3(G)], to yield the desired etch mask on an inclined plane. The experimental details of the process are described in the next sections.

## III. EXPERIMENTAL DETAILS

### A. Fabrication of the holder and sample size limitations

The holder shown in Fig. 3(A) was made from a standard *p*-type, boron doped, ⟨100⟩ oriented, double-sided polished silicon wafer with a thickness of 525 $\mu$m and a diameter of 100 mm. Slots were cut in the wafers using a Rofin-Sinar150 P2/CW YAG laser cutting machine using the settings shown in Table I. Care was taken not to align slots parallel to {110} crystal planes to avoid accidental breaking of the wafer. The walls of the slots are perpendicular to the wafer surface, which benefits in-plane placement of the samples with respect to the holder wafer surface. The length of the slots we used was 26 mm. The slots must be aligned radially with respect of the middle of the wafer to minimize the influence of the long sides of the samples on the resist thickness on the samples.

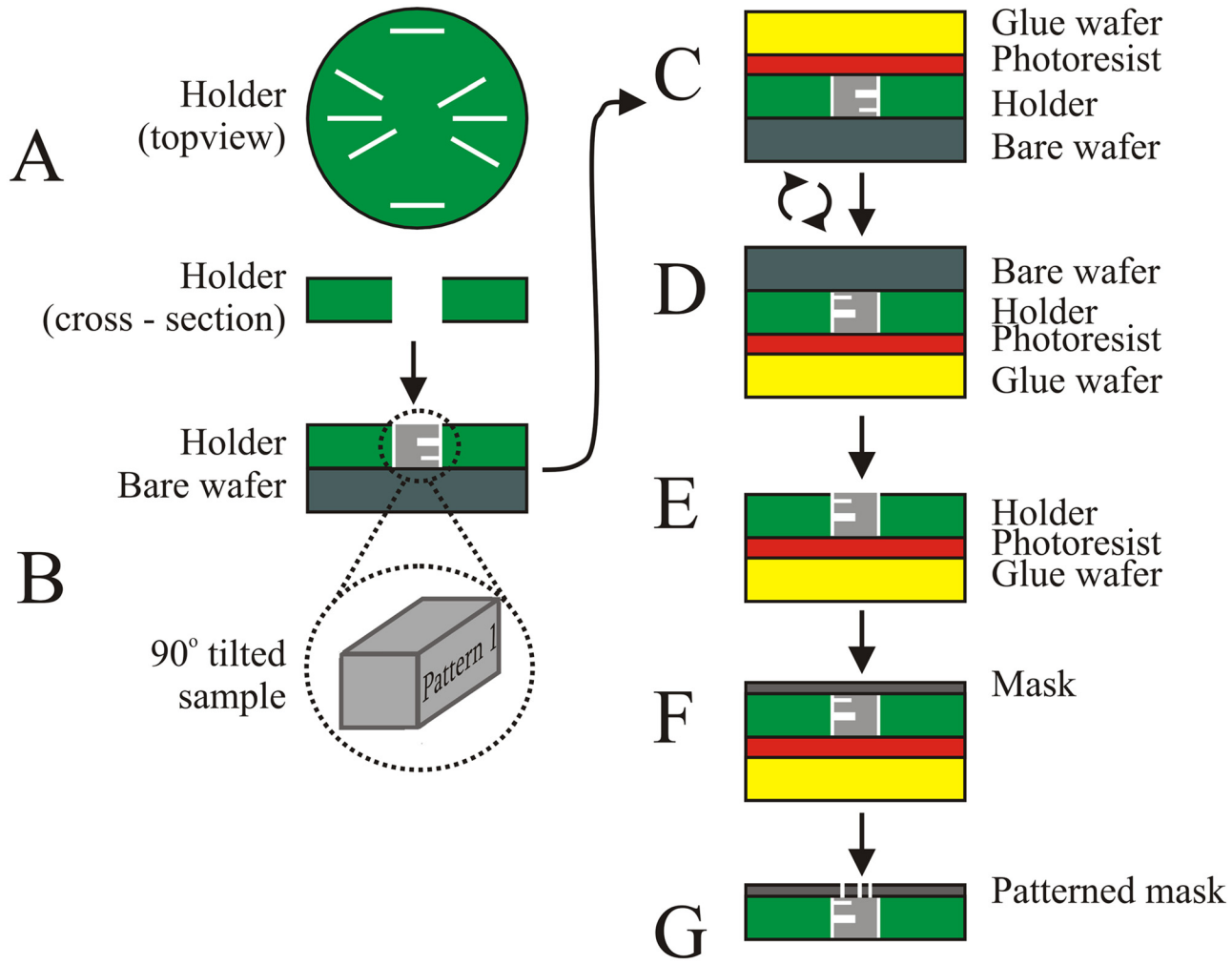


FIG. 3. (Color online) Process scheme using a holder to realize the patterning of a sample from two sides with standard clean room equipment. (A) The holder is made by etching slots in a silicon wafer. The slots are aligned oblique to the {110} crystal planes to avoid accidental breaking of the wafer. (B) The holder is placed on a flat, bare wafer, and the samples are placed in the slots in the holder. (C) The holder and sample are glued together by adding on top a third wafer with a thick layer of photoresist that acts as a glue. (D) After curing the photoresist, the wafer stack is flipped. (E) The bare wafer is removed. (F) An etch mask material is applied. (G) The etch mask material is patterned on an inclined plane.

After cutting the slots, the holder was covered by sputtered particles of silicon, ranging in size from approximately 50 $\mu$m to 300 $\mu$m. The largest excess particles were scraped off. Smaller particles were removed ultrasonically in water for at least 5 mins. Thereafter, the holders were immersed in an isotropically etching solution for 30 mins to etch away remaining silicon particles, see Table II. Afterwards, the wafers were rinsed with demineralized water and dried.

TABLE I. Overview of settings used during laser cutting of the slots in the holders. The slots were cut with a Rofin-Sinar 150 P2/CW YAG laser cutting machine.

| Setting | Value |
|---|---|
| Current to the laser | 100 A |
| Length of the laser pulse | 0.3 ms |
| Repetition frequency of the laser | 400 Hz |
| Spot size | 0.04 mm |
| Diaphragm | 1.5 mm |
| Cutting speed | 200 mm/min |
| Flow of $O_2$ delivered to the cutting area | 5 bar |

The maximum width of the sample is limited by the thickness of the holder to ensure that the sample sticks to the glue wafer and does not rise above the surface of the holder wafer during processing. In our case, the maximum width is limited to 525 $\mu$m. The maximum length of the sample is limited by photoresist spinning aspects. If photoresist is applied by spinning there are usually irregularities in the thickness of the resist near the beginning and end of the sample.[23] Therefore the samples must be longer than the structures that will be made in them, to ensure the presence of an area with a smooth layer of resist with the desired thickness. Here, we used samples with a length of 10 mm. Promising new technologies for the application of uniform photoresist layers are

TABLE II. Composition of the isotropic etching solution used to remove silicon particles from the holder.

| Compound | Fraction (vol. %) |
|---|---|
| 50% HF | 5 |
| 69% $HNO_3$ | 15 |
| $H_2O$ | 80 |

spray coating and electrodeposition.[23] Because no spinning is involved in these new technologies, the samples can have any shape or size, including cube-shaped samples.

### B. Preparation of the first nanostructure

Silicon wafers patterned with nanopores (pattern 1, see Fig. 2) were fabricated as described in Ref. 24. The pattern was a centered rectangular lattice of pores with lattice parameters $a = 680\,\text{nm}$, $c = 481\,\text{nm}$ ($a = \sqrt{2}c$), and radius $R = 210\,\text{nm}$. The pattern is intended as the (110) plane of a diamond crystal structure.[25] The fabricated sample is the first step in making a three-dimensional diamondlike photonic crystal with a band gap around 1500 nm. When made in a material with a high refractive index, photonic crystals can exhibit a photonic band gap: a frequency range for which light will not propagate because of multiple Bragg reflections.[15,16,24] The wafers containing pattern 1 were cleaved into pieces of approximately $10 \times 10\ \text{mm}^2$. The face of the sample in which pattern 2 was to be etched (see Fig. 2) was then polished parallel to the first set of pores to make the next process steps on the plane of the sample possible. To stabilize the etched pores in the two-dimensional crystal samples during polishing, a thick layer of photoresist (Olin 908/35) was deposited on the plane and in the pores, and cured overnight at 80 °C. The sample was then mounted in a tripod polisher (South Bay Technology)[26] and carefully polished. The polishing was performed using consecutively 30 $\mu$m, 15 $\mu$m, 9 $\mu$m, 6 $\mu$m, 3 $\mu$m, 1 $\mu$m, and 0.5 $\mu$m diamond lapping films. Initially the lapping film was rotating at 30 rpm, but as the lapping film was changed to smaller particle sizes, this speed was reduced to 10 rpm. When polishing with the final lapping film of 0.5 $\mu$m, the lapping film was not rotating, but the tripod polisher was carefully moved over the plane of the film without pressure. In all cases the direction of movement was parallel to the etched pores and never perpendicular. Polishing the samples provided a smooth surface that can be aligned perfectly in plane with the holder surface. After polishing, the two-dimensional crystal sample was rinsed. To remove the photoresist from the sample it was calcinated in an oven following the procedure outlined in Table III.

After polishing, the samples were glued to plastic foil with the polished side perpendicular to the foil, and cut to typical dimensions of $10 \times 0.5 \times 0.4\ \text{mm}^3$ using a Disco DAD-321 dicing saw equipped with a NBC-Z-2050 blade. The thickness of the slices was intentionally made a few $\mu$m thinner than the measured thickness of the holder to prevent the samples from reaching above the backplane of the holder in subsequent steps. After dicing the samples and removing the foil, the samples were cleaned by immersion in acetone, rinsing, and subsequent heating in an oven using the procedure shown in Table III to remove all organic contaminants.

TABLE III. Overview of the calcination procedure used to remove photoresist from the samples.

| Step | Description |
|---|---|
| 1 | From room temperature to 80 °C at 20 °C/hour |
| 2 | Hold 80 °C for 60 minutes |
| 3 | From 80 °C to 650 °C at 120 °C/hour |
| 4 | Hold 650 °C for 360 minutes |
| 5 | Cool down to 25 °C in six hours |
| 6 | End program |

### C. Application and patterning of the chromium etch mask on the second, inclined plane

To mount the samples, a holder was placed on top of the bare silicon wafer [Fig. 3(b)]. The samples were placed in the holder with the polished plane that was to be structured further on the bottom. This polished plane is therefore aligned in-plane with the holder wafer surface and will eventually receive an etch mask with pattern 2. To fix the samples in place, a thick layer of photoresist (Olin 908/35) was deposited on a separate double side polished 100 mm silicon wafer, by spincoating at 1500 rpm for 30 seconds. Using photoresist to bond wafers in a stack is common in standard microfabrication, see for example.[27] However, in order to properly fix the sample in the holder wafer, a much thicker layer of photoresist than normal was spincoated. The spincoating was done at room temperature with photoresist that was kept at 7 °C until just before the experiment, to ensure that the resist was still highly viscous when it was applied to the wafer. In this way a layer was formed that was sufficiently thick to fill small gaps between the sample and the glue wafer, but not so thick that it leaked from the sides of the stack. The glue wafer that was fabricated in this way was placed on top of the holder containing the samples, thereby connecting samples, holder and glue wafer. The resulting stack was pressed together by a 0.5 kg weight, and held overnight in an oven at 80 °C to cure the photoresist. After flipping the entire wafer stack, the bare wafer was removed. The planes of the holder and of the samples therein were cleaned by a 5 min exposure to oxygen plasma from a Tepla 300 E dry etcher, using the settings shown in Table IV. Subsequently, the plane was coated with a 50 nm thick chromium layer using electron gun evaporation on a Balzers BAK 600.

In this work, we chose pattern 2 to be the same pattern as the pattern 1 that was used to obtain the first nanostructure in order to realize a diamond structure.[25] A critical requirement to obtain a diamond-structured photonic crystal with a large photonic band gap is that the second pattern is carefully aligned with respect to the first pattern, such that the centers of the holes in the chromium etch mask are centered between the axes of the pores of pattern 1.[29]

The chromium etch mask layer on the samples can be patterned using e-beam-, laser interference-, or deep UV lithography and subsequent etching. Another option for patterning

TABLE IV. Overview of settings used during cleaning of the wafer plane using oxygen plasma from a Tepla 300 E dry etcher.

| Setting | Value |
|---|---|
| Plasma power | 300 W |
| $O_2$ flow (mass flow controller) | 50% |
| Pressure | 1.25 mbar (typically) |

the chromium etch mask is the use of a focused ion beam. We opted for the latter method because of our familiarity with this technique. To prevent charging of the sample by the ions, a good electrical connection between the samples and the glue wafer was provided by used a 25 $\mu$m thick aluminum wirebond connecting the samples to the holder, and the holder to the glue wafer underneath. The wire was fixed to the sample and holder using a Marpet Enterprise MEI 1204 W wire bonding apparatus.

The combination of glue wafer and holder was mounted in a FEI $\times$ T Nova Nanolab 600 Dual Beam workstation, using a metal 4" wafer holder. An array of approximately $8 \times 6\ \mu m^2$ containing the desired pattern of holes was milled in the chromium at 30 kV and 93 pA. This array was aligned to the existing pores in the sample by use of the *in situ* imaging functionality of the FIB workstation. The magnification of the focused ion beam machine was adjusted to ensure the pores in the two orthogonal directions had exactly the same lattice spacing. The pattern was milled for approximately 75 seconds. After characterization by scanning electron microscopy, the wafer stack was removed from the focused ion beam milling equipment. The chromium etch mask could now be used to make the second set of pores. The whole process of making an etch mask for the fabrication of three-dimensional structures in the way described here takes approximately 13 work days. The same deep reactive ion etching process that was applied for etching the first set of pores[24] was used to etch the second set of pores.[30]

## IV. RESULTS AND DISCUSSION

### A. Preparation of the samples containing the first nanopattern of pores

Figure 4(A) shows a side view of a cleaved sample that contains the first pattern, which in our case is a set of nanopores as described in Refs. 25 and 29. The sample has been

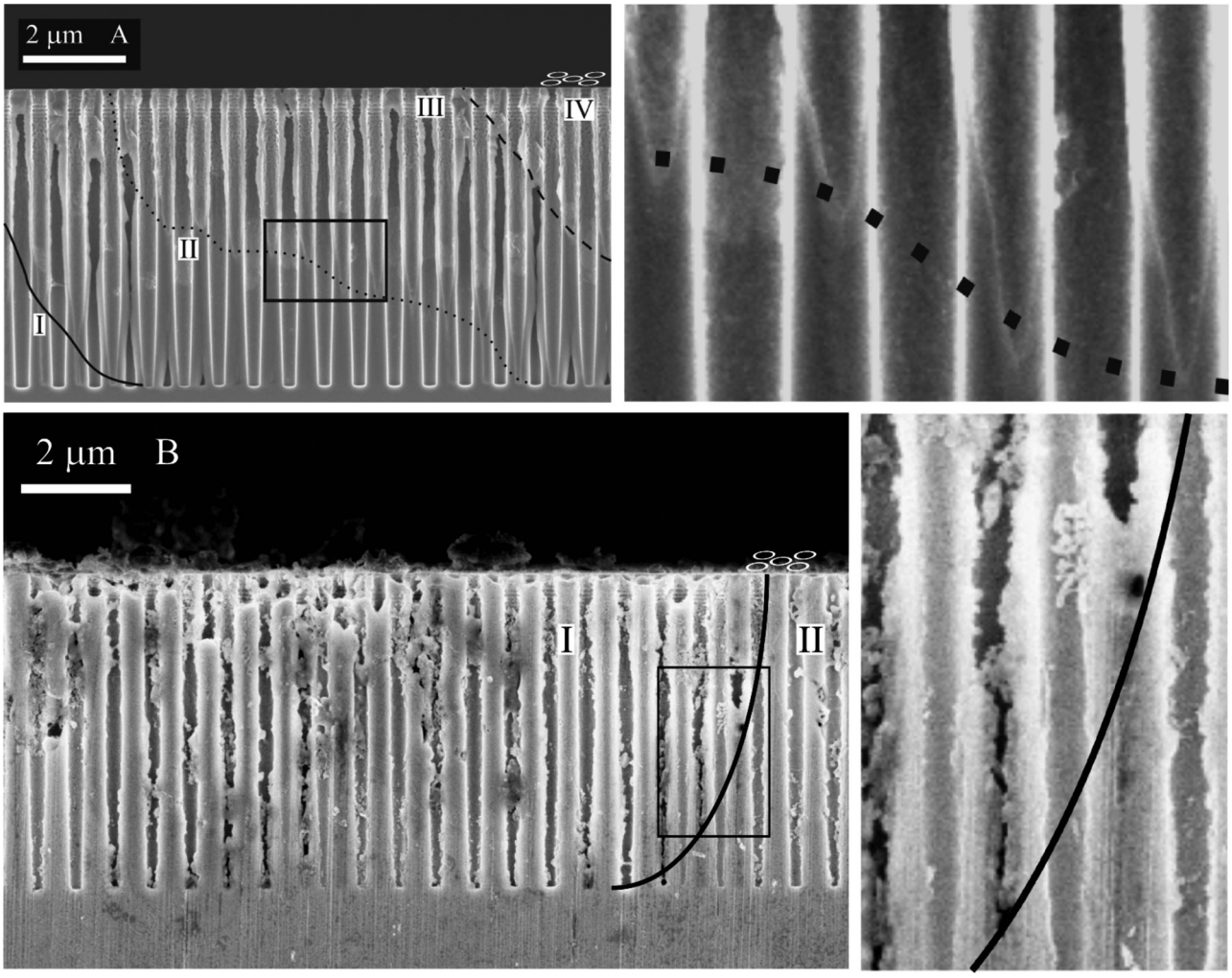


FIG. 4. (A): Scanning electron micrograph of a cleaved array of deep pores that were etched in the pattern of the first nanostructure, before polishing. The symbols I-IV indicate surface levels that are at different heights, separated by the distance between two closest pores in the sample. The surface steps that separate the different levels are indicated with curves. The steps appear due to the cleaving of an already nanostructured material. A zoom-in of the area indicated by the rectangle is shown on the right. The contrast is enhanced to show pores running along the surface from top to bottom. The pores 'vanish' at the positions indicated by the curves. (B): Scanning electron micrograph of cleaved deep pores after polishing. The long-range roughness of the sample has decreased: I and II indicate only two remaining surface levels separated by one step. As a result of the polishing the edges of the pores have become ragged. Small particles are seen in the pores. These particles are removed during the patterning of the etch mask in the inclined plane. On the right a close-up of the area indicated by the rectangle can be seen.

cleaved through the pores, which are visible on the cleavage plane. Although the plane looks very smooth, "steps" with a height of 0.5 $c$ (here 240 nm) appear on the plane, indicated by the lines that serve as guides to the eye. These lines indicate locations on the sample surface where pores 'disappear' into the bulk of the sample, yielding a crystallograpic step on the surface. These surface steps may cause the sample to lie at an angle on the bare wafer, which has a detrimental effect on the quality of structure after the second etching step. For instance, a misalignment of the second etching direction is undesirable for photonic crystals, because it would result in a narrower photonic band gap.[28,29] To reduce the effects of misalignment so as to reach the high demands we set on the mutual alignment of inclined nanostructures, the cleaved plane was polished.

Figure 4(B) shows a sample with similar pores, after polishing. It can be observed that the steps on the plane have been almost completely removed. Now the plane is smooth enough to be able to align the two nanostructures with respect to each other with the required accuracy. Figure 4(B) also shows small particles in the pores after polishing. We believe these nanoparticles to be silicon particles from the sample and diamond particles from the lapping film. Fortunately, these particles are etched away while making the second nanostructure. We expect that the influence of the particles on the function of an integrated device as shown in Fig. 1 will be minor: the particles will be oxidized and covered with a nonconducting silica layer. Therefore their conductivity is low. Also, when nonporous surfaces are polished they will reveal much fewer particles than our porous samples. We conclude that polishing the sample before applying and patterning the second etch mask on an inclined plane greatly improves the quality of the final three-dimensional structure.

## B. Mounting the sample in the holder

A scanning electron micrograph of a sample mounted in the holder is shown in Fig. 5. The figure clearly shows the opening in the holder that has rough sides as a result of the laser cutting. Fortunately, this roughness does not affect the further processing. The wire bond that was made to enable the patterning of chromium by focused ion beam is also visible and appears to be properly connected.

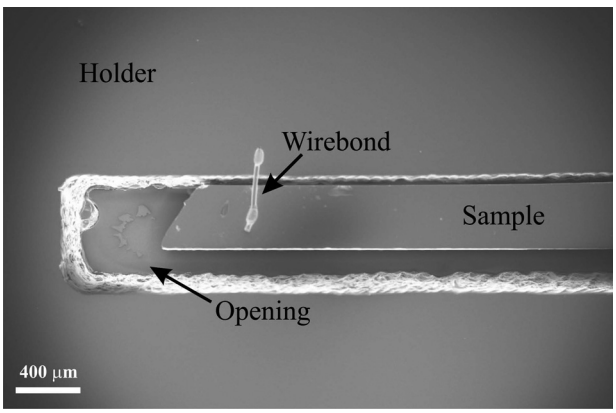


FIG. 5. Scanning electron micrograph of a sample glued in a slot in the holder [compare Fig. 3(E)]. The rough edges of the slot in the holder do not hamper the alignment. The wire bond, which is in excellent condition, ensures a good electrical connection between the sample and the holder. This connection enables patterning using a focused ion beam.

## C. Application and patterning of the chromium etch mask on the second, inclined plane

Figure 6 shows a scanning electron micrograph of a silicon wafer that has been successfully patterned on two inclined planes. The upper half of the image shows the first pattern in the ($y$, $z$) plane, that has been etched deeply into the silicon using reactive ion etching. The lower half of the image shows the second pattern in the ($x$, $y$) plane of the sample, that consists of holes milled in a layer of Cr. This will act as a hard etch mask for subsequent etching. The figure clearly shows that the particles seen in Fig. 4(B) are etched away. The second pattern extends over an area of $6.4 \times 9.6\,\mu m^2$ or $14 \times 13$ unit cells. The size of the pattern is limited by the focused ion beam equipment we used, and can be greatly extended by the use of e-beam-, laser interference- or deep UV lithography and subsequent etching. At any rate, the size of these structures is sufficiently large to successfully obtain functional nanophotonic structures.[31,32]

Figure 6 illustrates the success of our method. The hole centers of the second pattern are aligned very well between the centers of the pores of the first pattern. To quantify the alignment accuracy, we determined the deviation $\Delta y$ from perfect alignment. The deviation was determined by measuring the displacement $\Delta a_y$ between the unit cells of the two separate planes. The displacement $\Delta a_y$ for each unit cell was measured along the edge of the sample, which is parallel to the $y$-axis and the long lattice spacing $a$ of the unit cells. In case of perfect alignment, the displacement is equal to

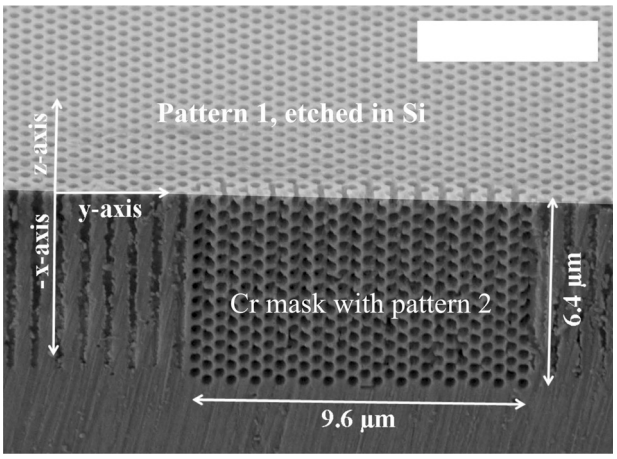


FIG. 6. Scanning electron micrograph of a chromium etch mask on an inclined plane of a silicon sample. The chromium layer was patterned by a focused ion beam. The hole centers of the second nanostructure are intentionally positioned at a distance of $\Delta a_y = (1/4)a$ with respect to the first nanostructure, of which some pores are clearly seen (parallel to the ***x***-axis). In this case, the accuracy of the alignment of the pattern for the second nanostructure with respect to the first nanostructure is $\Delta y = -15.2 \pm 14.7$ nm. At this step of the process, the small particles shown in Fig. 4(B) have vanished. The scale bar equals 5 $\mu$m.

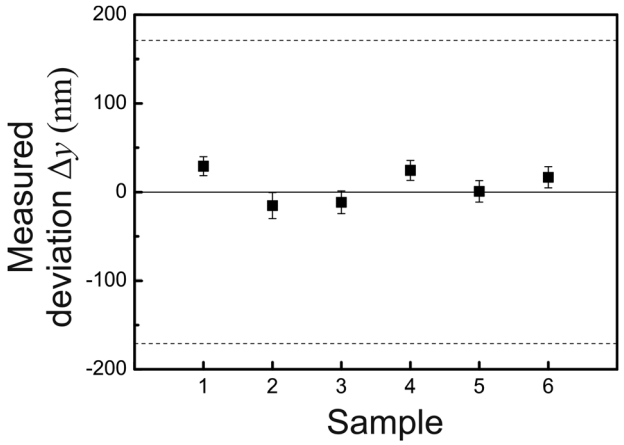


FIG. 7. Measured deviation $\Delta y$ for six fabricated samples. The measured deviations are centered around $\Delta y = 0$ nm. The smallest observed deviation is equal to $\Delta y = 1 \pm 12.1$ nm. The largest deviation is $\Delta y = 29.2 \pm 10.6$ nm. The dashed lines are at $\Delta y = +(1/4)a$ and $\Delta y = -(1/4)a$, which are the extreme deviations for which the centers of the pores in the two arrays would overlap. In case of perfect alignment the deviation is equal to $\Delta y = 0$ nm.

$\Delta a_y = (1/4)a = 172$ nm. The deviation $\Delta y$ is equal to the difference between the measured and the perfect value for the displacement:

$$\Delta y = \frac{1}{4}a - \Delta a_y.$$

Because the displacement could occur in the positive- as well as in the negative $y$ direction $\Delta y$ could be positive or negative. We found that in the sample presented in Fig. 6 the two pore sets were excellently aligned with a deviation of only $\Delta y = -15 \pm 15$ nm. In order to estimate a typical alignment accuracy, we measured the achieved precision for six of our samples. The measured deviations are shown in Fig. 7. The best structure has a deviation from perfect alignment of only $\Delta y = 1 \pm 12$ nm. The largest deviation that was observed is $\Delta y = 29 \pm 11$ nm, which is of the order of the diameter of the focused ion beam. The reported deviations are consistent with what one can reasonably expect to achieve with this prototyping technique. Considering these small deviations from perfect alignment, and neglecting other deviations such as tapering of the pores or rotational deviations, a design study predicts that the width of the photonic band gap remains more than 90% compared to a photonic crystal with perfect alignment.[28,29]

For one of our structures we have also managed to determine the rotational deviation of the orientation of the second structure. This is the angle between the pattern that was milled in the chromium etch mask material, and the edge of the plane in which the first structure is etched. This angle was determined to be $0.71 \pm 0.24°$. The observed small rotational deviation is not expected to significantly reduce the properties of fabricated photonic crystals.[29]

## V. CONCLUSIONS

We have developed a method to apply and pattern etch masks on several inclined planes using CMOS compatible nanofabrication technology. As a demonstration of the applicability of the method, we have fabricated a pattern in a chromium etch mask that was deposited on a 90° plane, perpendicular to the plane of a wafer that already contained an array of deep nanopores. The chromium was patterned using a focused ion beam. We have chosen a pattern equal to the pattern that was used for etching the pores in the first direction. We have determined the alignment- and rotational accuracy of our method, and found them to be better than $\pm 30$ nm and $\pm 0.71°$, respectively, which is at the limit of the accuracy of the equipment used.

While we have chosen to pattern the second etch mask equal to the first in order to realize three-dimensional silicon photonic bandgap crystals, it is evident that our method allows for different and arbitrary patterns to be combined. The achievement described in this article opens the road to a great variety of novel three-dimensional nanostructures. Therefore, our method allows for exciting potential applications in the fabrication of new three-dimensional devices in, i.e, microfluidics, photonics, and three-dimensional silicon electronics.

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